RIGOL

Clock Recovery

Advanced Feature for Oscilloscopes

Application Note

May, 2026

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Contents

1. Document Overview

This document is designed to introduce the clock recovery feature of RIGOL's oscilloscopes. The contents include:

- Basic concepts and working principles of clock recovery;
- How to use the clock recovery feature on the oscilloscope;
- Test procedures for performing clock recovery on the typical high-speed serial digital signals.

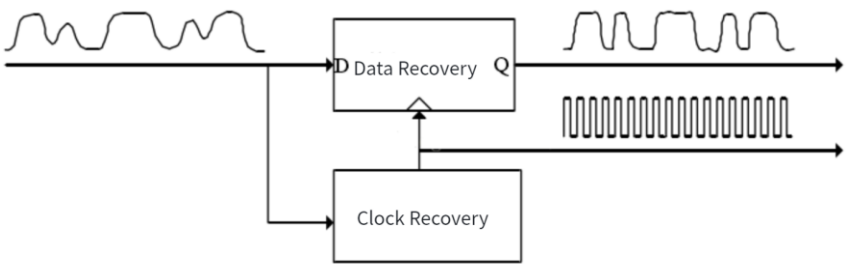
This document is intended for engineering technicians who need to perform the clock recovery test for the high-speed serial digital signal on an oscilloscope. For the clock recovery feature of the oscilloscope and the relevant product manuals of the oscilloscope, log in to the official website of RIGOL (www.rigol.com) to download them.

2. Clock Recovery Overview

In the high-speed signal testing, clock recovery is a prerequisite for the oscilloscope to perform eye diagram analysis, jitter measurement, and other measurements for the evaluation of the signal integrity.

Since most high-speed serial digital communications lack an independent clock signal, clock information is inherently embedded in the data transitions. If the oscilloscope fails to obtain an accurate clock to sample the signal, there will be a rate mismatch and phase deviation between the clock and the data, which will lead to misinterpretation of the data sampling (such as a 0/1 level misreading), and it is impossible to effectively evaluate the timing consistency of signal edges.

Clock Recovery, also known as Clock and Data Recovery (CDR), is a process of extracting clock signals from the serial data stream and sampling data on a timing basis to recover the raw data. The schematic diagram is as follows:



CDR Diagram

The oscilloscope generally provides the following clock recovery methods:

- **PLL**

Dynamically tracks data phase/frequency, applicable for high-speed complex signal analysis. You are required to make a precise configuration of parameters to filter out specific high-frequency jitter. It is suitable for high-speed bus and protocol compliance

test.

- **Constant**

Based on preset symbol rate to fit the clock; remove low-frequency jitter with the low-pass filter to output the synchronous clock without low-frequency interference, suitable for medium-low-speed signal jitter analysis.

- **Explicit**

Directly inputs external sync clock as the basis to complete data recovery, featuring fast response and no internal error, relying on external clock scenarios, only suitable for high-precision test of source synchronous signals.

3. Clock Recovery Feature

RIGOL's oscilloscopes allow the user to select a variety of clock recovery methods based on their actual scenarios and extract clock information from the serial data. The clock recovery feature also provides accurate clock signals for the oscilloscope to perform "jitter measurement", "jitter decomposition measurement" and "eye diagram analysis" to complete these complex measurements and signal analysis.

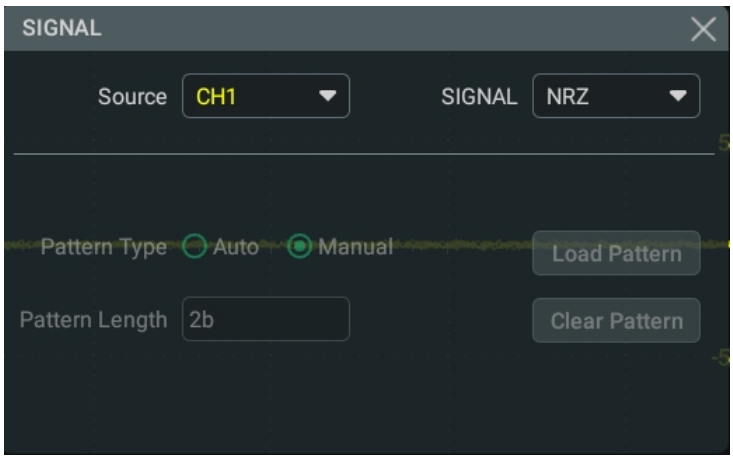
The clock recovery test operation involves the following three function menus:

- Signal Type
- Threshold
- CDR

Click or tap the function navigation icon  at the lower-left corner of the screen to open the function navigation. Then, click or tap the specified function menu to enter the specified function setting interface.

3.1 Signal Type

Used to set the type of signal under test. For a different selection of the signal type, threshold, and parameter configuration settings, the settings for the clock recovery parameters and clock recovery process are different. The signal type interface is displayed in the following figure.



3.1.1 Source

Selects the input channel to which the current signal under test is connected based on the actual test signal connection.

3.1.2 Signal Type

Selects the code type of the signal under test.

- **NRZ**

  NRZ (Non-Return-to-Zero) is the most basic binary encoding which adopts logic "1" and logic "0" to indicate two levels (high level/low level), respectively. 1-bit information is transmitted per symbol period.

  It is applicable to low-speed, short-range, and high-reliability signal transmission. For example, On-die, industrial control, etc.

- **PAM3**

  PAM3 (Pulse Amplitude Modulation 3, 3-Level Pulse Amplitude Modulation) employs three distinct voltage levels (e.g., -1, 0, +1 or 0, 1, 2) for ternary encoding. It transmits approximately 1.58 bits of information ($\log_2 3$) per symbol period, delivering a bandwidth efficiency improvement of roughly 58% compared with traditional NRZ bandwidth.

  It is suitable for medium-to-high speed transmission scenarios where there is a high requirement for the costs, performance, and anti-interference.

- **PAM4**

  PAM4 (Pulse Amplitude Modulation 4, 4-Level Pulse Amplitude Modulation) employs four distinct voltage levels (representing 00, 01, 10, and 11) for quaternary encoding. It transmits 2 bits of information per symbol period, effectively doubling the bandwidth efficiency compared with the traditional NRZ.

  It is applicable to high-speed, ultra-high-speed communication scenarios, such as optical communication, data center, etc.

3.1.3 Other Setting Parameters

The following items are parameter settings related to jitter decomposition. As for the clock recovery feature, these items do not need to be set. This document will not elaborate on them in details.

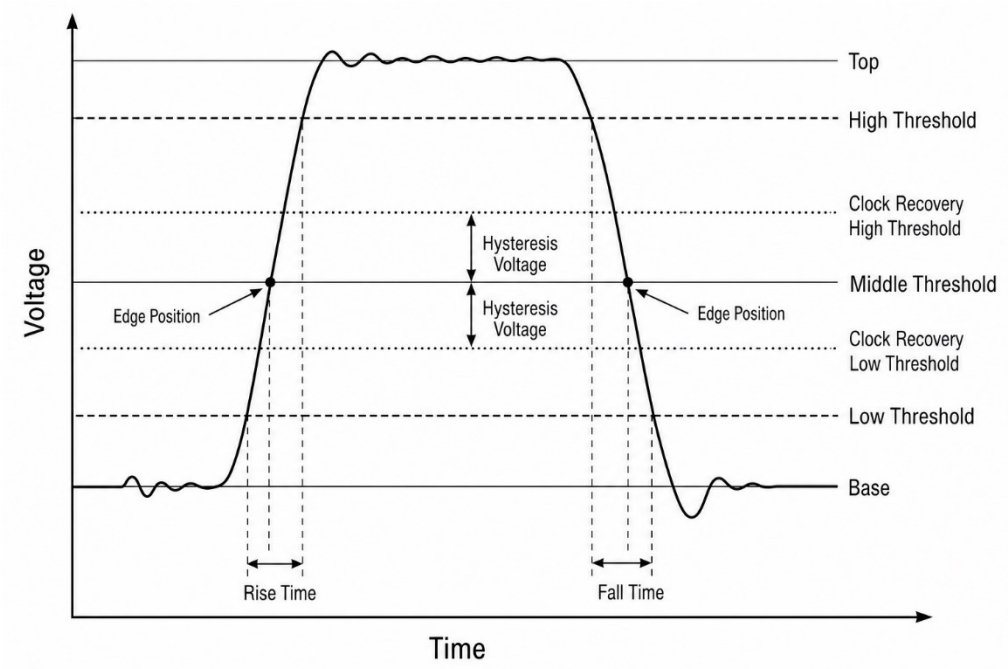
- Signal Type
- Pattern Length
- Load Pattern
- Clear Pattern

3.2 Threshold Settings

For the clock recovery feature, threshold settings are used to enable the oscilloscope to accurately identify the effective edge of the input signal and thus reliably extract the clock signal synchronized with the input signal.

3.2.1 Definition of Threshold Parameters

The following figure takes the NRZ signal as an example to illustrate how the threshold is defined between the TOP and BASE levels.



The main parameters associated with clock recovery are the "Middle Threshold" and the "Hysteresis Voltage".

- **Middle Threshold**

  The middle threshold is usually the midpoint of the high level (Top) and low level (Base), and it is used as the time reference for edge detection.

  - When a signal level is detected to pass from low level to the middle

threshold, a rising edge is judged to be coming.

- When a signal level is detected to pass from high level to the middle threshold, a falling edge is judged to be coming.

The rising or falling edge of the recovered clock will be precisely aligned to the mid-threshold crossing point, so the accuracy of the mid-threshold setting directly affects the phase accuracy of the recovered clock.

- **Hysteresis Voltage**

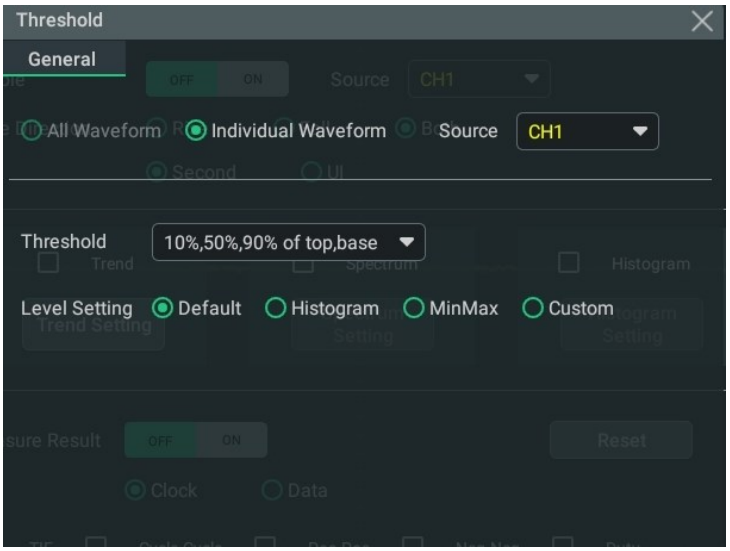
To avoid minor fluctuations or noise on the signal being mistaken for a valid edge, a "buffer zone" is set up for edge detection. As shown in the figure above, the hysteresis voltage is the difference between the "Clock Recovery Low Threshold " and the "Clock Recovery High Threshold". This region is the hysteresis voltage band.

- When a signal level is detected to rise from below the " Clock Recovery Low Threshold" to above the middle threshold, it is judged as a valid rising edge.
- When a signal level is detected to fall from above the "Clock Recovery High Threshold" to above the middle threshold, it is judged as a valid falling edge.

The hysteresis voltage effectively filters out jitter and noise superimposed on the signal, avoiding glitches on the recovered clock.

The threshold definitions for PAM signals are similar, and will not illustrate it here.

3.2.2 Threshold Settings for the NRZ Signal



3.2.3 Input Signal

- **All Waveforms/Individual Waveform**
  - All Waveforms: The current threshold and level settings are applicable to

all the waveforms.

➢ Individual Waveform: The current threshold and level settings are only applicable to the individual waveform of the currently selected source. By default, Individual Waveform is selected.

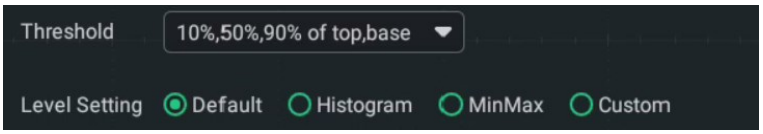
- **Source**

If you select "Individual Waveform", you need to select the input channel of the signal under test. By default, CH1 is selected.

3.2.4 Threshold Settings

The NRZ signal supports the following 5 threshold settings:

- **10%, 50%, 90% of top, base**



The threshold is expressed in percentage, with the fixed threshold settings: Low threshold (10%), Middle Threshold (50%), and High Threshold (90%).

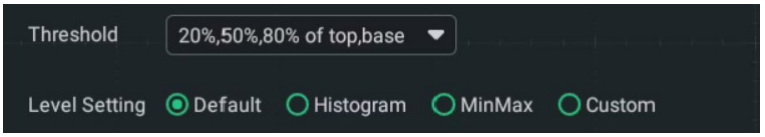
V_Top and **V_Base** are voltages of Top level and Base level, which can be obtained through the "Level Setting" calculation.

Middle Threshold = (**V_Top + V_Base**)***Percentage**

Hysteresis Value = (**V_Top - V_Base**)***40%**

Application Scenario: Test the standard NRZ signals (e.g. protocol compliance test, etc.)

- **20%, 50%, 80% of top, base**



The threshold is expressed in percentage, with the fixed threshold settings: Low threshold (20%), Middle Threshold (50%), and High Threshold (80%).

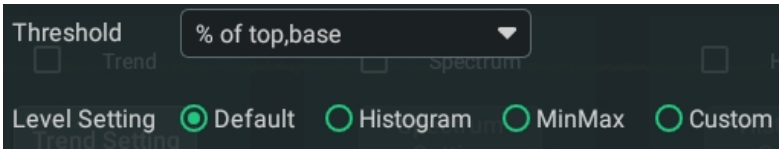
V_Top and V_Base are voltages of Top level and Base level, which can be obtained through the "Level Setting" calculation.

Middle Threshold = (V_Top + V_Base)*Percentage

Hysteresis Value = (V_Top - V_Base)*30%

Application Scenario: Test the signal with degraded slew rates (e.g., attenuated signal after long-range transmission)

- **% of top, base**



The threshold can be set to:

Low threshold (Default 10%), Middle Threshold (Default 50%), and High Threshold (Default 90%).

V_Top and **V_Base** are voltages of Top level and Base level, which can be obtained through the "Level Setting" calculation.

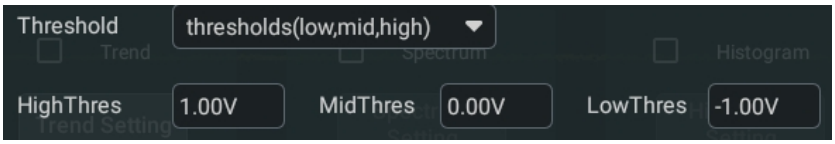
Middle Threshold = (V_Top+V_Base)*user-defined percentage

Upper Hysteresis = (V_Top-V_Base)*(High Threshold – Middle Threshold)

Lower Hysteresis = (V_Top-V_Base)*(Middle Threshold – Low Threshold)

Application Scenario: Test the non-standard NRZ signals

- **thresholds (low, mid, high)**



Users can set the thresholds directly.

Low threshold (Default -1.00V), Middle Threshold (Default 0.00V), and High Threshold (Default -1.00V).

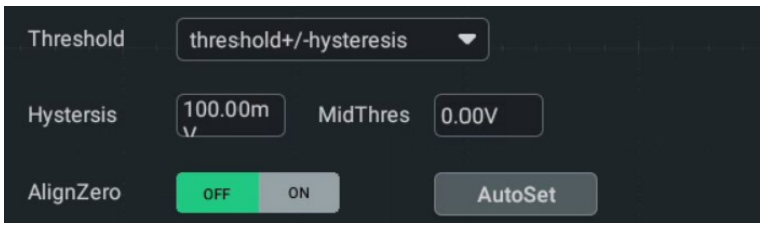
V_Top and **V_Base** are the voltages of "High Threshold" and "Low Threshold".

Upper Hysteresis = (High Threshold Voltage – Middle Threshold Voltage)

Lower Hysteresis = (Middle Threshold Voltage – Low Threshold Voltage)

Application Scenario: Known signal level standards (e.g., signals with fixed 3.3V logic)

- **threshold+/-hysteresis**



Users can set the "Middle Threshold" and "Hysteresis" directly.

Align Zero: By default, it is disabled. When it is enabled, the oscilloscope will automatically align the middle threshold to 0 V.

AutoSet: when you click or tap this menu, the oscilloscope automatically sets the middle threshold and hysteresis voltage.

Middle Threshold = (V_Top+V_Base)*50%

Hysteresis Voltage = (V_Top-V_Base)*5%

Application Scenarios: Scenarios where precise phase control is required (e.g., test that imposes a high requirement for clock synchronization)

3.2.5 Level Setting

The level setting is used to select how each level voltage is calculated and directly affects the value of each threshold voltage.

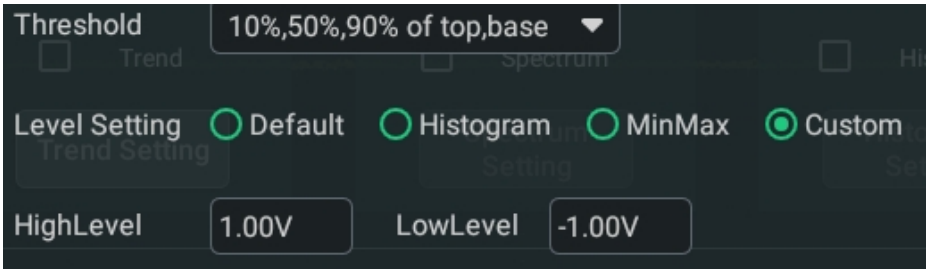
"Level Setting" is required to be set when the threshold is set to the following 3 modes.

10,50%,90% of top, base

20,50%,80% of top, base

% of top, base

The **Level Setting** menu has the following options:



- **Default**

  The oscilloscope automatically selects "Histogram" or "MinMax" based on the characteristics of the signal under test to calculate the high level (V_Top) voltage and low level (V_Base) voltage.

Tips:

For some signals, for example, a Sine wave, when you select "Default", the level setting may switch between "Histogram" and "MinMax" mode. At this time, we recommend you to set the level setting to "Histogram" or "MinMax" to ensure the stability of the results.

Application Scenario: Tests the standard NRZ signals (without noise).

- **Histogram**

  By analyzing the histogram distribution of signal voltages (the probability of the occurrence of different voltages), the "high-level range" and "low-level range" with the highest probability are identified to determine V_Top (typical of the high-level range) and V_Base (typical of the low-level range).

  Application Scenario: Tests the signal with random noise and with small fluctuations in level.

- **MinMax**

  The oscilloscope sets the maximum voltage value of the signal under test to high level (V_Top) and the minimum voltage value to low level (V_Base).

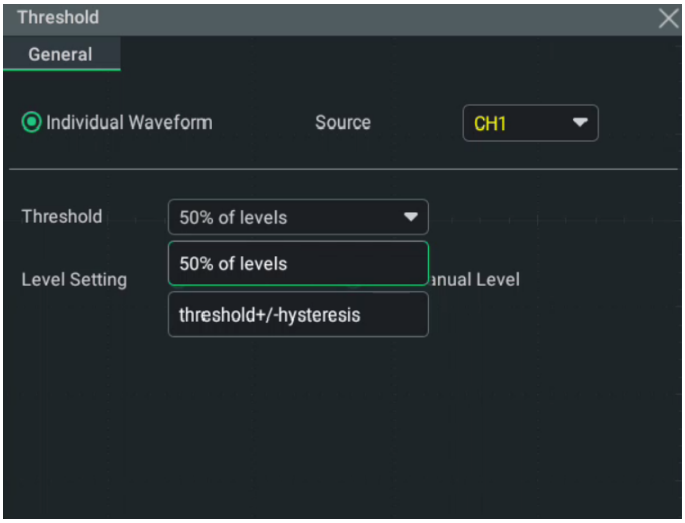
Application **Scenario**: Measures the signal with clear edges and minimal noise.

- **Custom**

  Sets the user-defined voltages of high level (V_Top) and low level (V_Base).

  Application Scenario: Tests the standard NRZ signals with the known level.

3.2.6 Threshold Settings for the PAM Signal



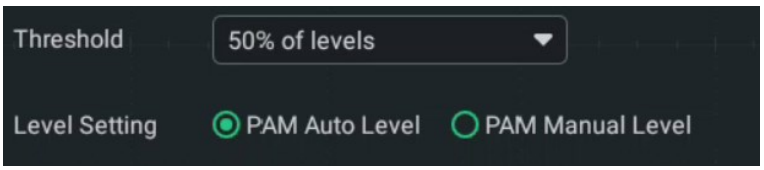
3.2.6.1 Input Signal

The threshold settings for the PAM signal are only available for the individual waveform. You need to select the input channel of the signal under test. By default, CH1 is selected.

3.2.6.2 Threshold Settings

The PAM (pulse amplitude modulation) signals are multi-level encoded (e.g. PAM3 is 3-level and PAM4 is 4-level), so the transition between the adjacent levels is required. Two threshold settings are available:

- **50% of levels (automatic threshold mode based on mid-point level)**



The midpoint of the two adjacent level voltages is used as the threshold to distinguish the level transition.

Item	PAM3	PAM4
Encoding	3-level (V0, V1, V2)	4-level (V0, V1, V2, V3)

Level		
Adjacent Level Decision Threshold	V0→V1: (V0 + V1) x 50%	V0→V1: (V0 + V1) x 50%
	V1→V2: (V1 + V2) x 50%	V1→V2: (V1 + V2) x 50%
		V2→V3: (V2 + V3) x 50%

Set or obtain the level value in "Level Setting".

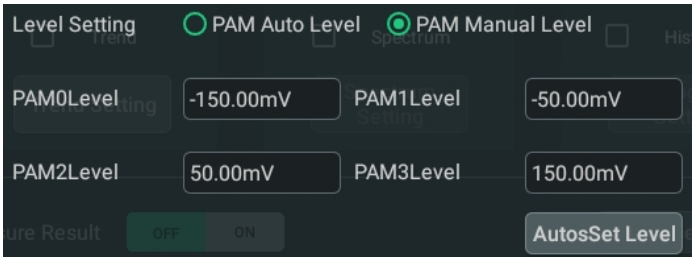
- The hysteresis value of the PAM3 signal is defined as 3% of the adjacent level difference.
- The hysteresis value of the PAM4 signal is defined as 2% of the adjacent level difference.

- **threshold+/-hysteresis**

Sets the threshold and the hysteresis manually.

- Hysteresis: indicates the hysteresis voltage value.
- PAM01 Threshold: decision threshold voltage between V0 and V1.
- PAM12 Threshold: decision threshold voltage between V1 and V2.
- PAM23 Threshold: decision threshold voltage between V2 and V3 (only available for PAM4 signals).
- AutoSet: when you click or tap this menu, the oscilloscope automatically sets the threshold and hysteresis value for each threshold.

3.2.6.3 Level Setting



The level setting is required when the threshold setting for the PAM signal is "**50% of levels**".

- **PAM Auto Level**

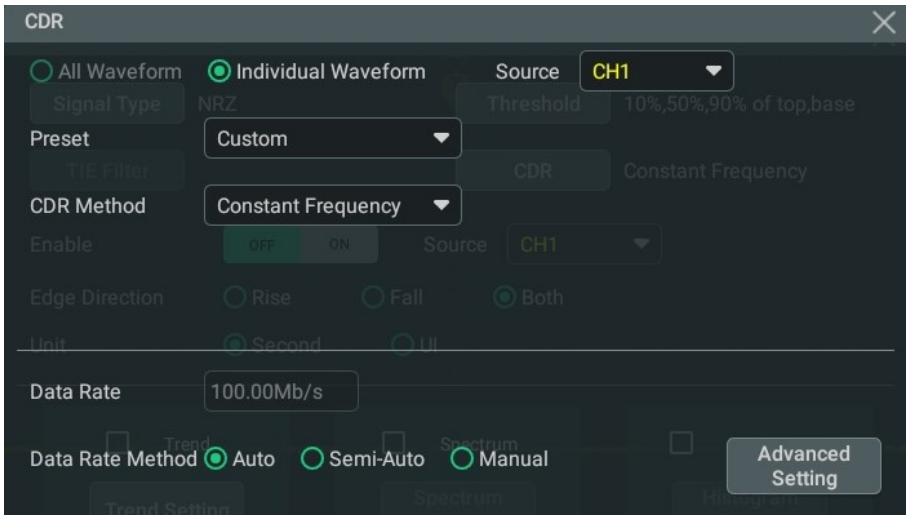
The oscilloscope automatically calculates the voltage values for each level of the PAM signal in the voltage histogram.

- **PAM Manual Level**

  The voltage of each level of the PAM signal can be set by the user manually. You can also click or tap **AutoSet Level** to set the level voltage automatically.

3.3 Clock Recovery Setting

The oscilloscope's clock recovery feature supports 4 kinds and 8 methods of clock recovery. The settings are identical for the NRZ and PAM signal type, but additional parameter settings are required for the clock recovery setting for the PAM signal.



- **All Waveforms/Individual Waveform**

  All Waveforms: configures the same clock recovery parameter settings for the waveforms of all the channels.

  Individual Waveform: configures the clock recovery settings for the selected single source channel.

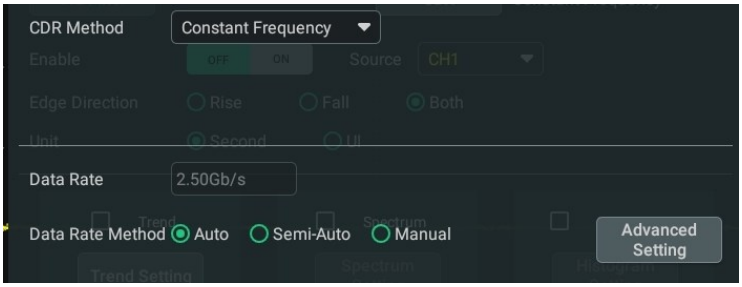
- **Source**

  If you select "Individual Waveform", you need to select the source channel of the waveform under test. By default, CH1 is selected.

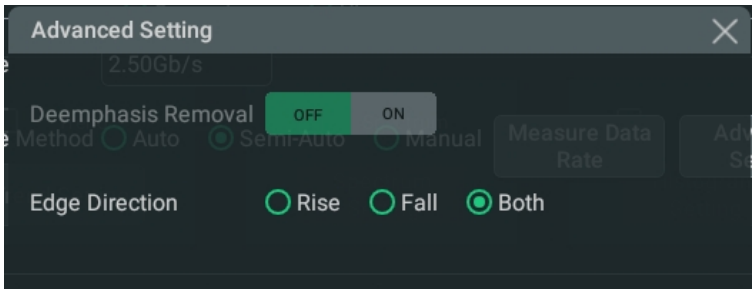
- **Preset**
  Presets the clock recovery method for various protocols. You can select the preset clock recovery method based on your test requirements.

3.3.1 Constant Frequency

Recovers the clock signal based on a constant clock frequency. When you select Constant Frequency, the following configuration interface is displayed.



- **Data Rate Method**
  - **Auto:** The oscilloscope automatically measures the data rate of the signal under test and performs clock recovery based on the measurement result.
  - **Semi-Auto:** Inputs the "Data Rate" value as a reference, and then click or tap **Measure Data Rate** to measure the data rate of the signal under test. In this way, the data rate is generally more accurate. The oscilloscope performs clock recovery at this rate.
  - **Manual:** recovers the clock by the data rate that you input manually.
- **Advanced Setting**



  - **Deemphasis Removal** (Not available currently)
  - **Edge Direction**

Rise: only uses the rising edge of the signal under test for clock recovery.

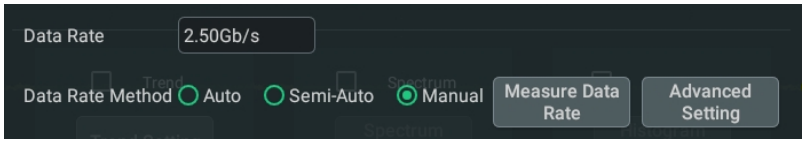
Fall: only uses the falling edge of the signal under test for clock recovery.

Both: It is the default edge direction. Both the rising and falling edges of the signal under test are used for clock recovery.

3.3.2 PLL

Phase-locked loop clock recovery includes first-order/second-order/third-order phase-locked loop clock recovery, slightly different in the configurations for each type.

3.3.2.1 Common Setting



- **Data Rate**

  You can set the expected data rate for the signal under test.

- **Measure Data Rate**

  Click or tap **Measure Data Rate**, and the oscilloscope automatically tests the data rate of the signal under test.

Tips:

When measuring a NRZ signal with unknown data rate, you should maximize the sample rate, optimize the vertical scale of the signal to make its amplitude take up the display area. Set the memory depth to Auto and maximize the acquisition time to ensure the accurate calculation of data rate.

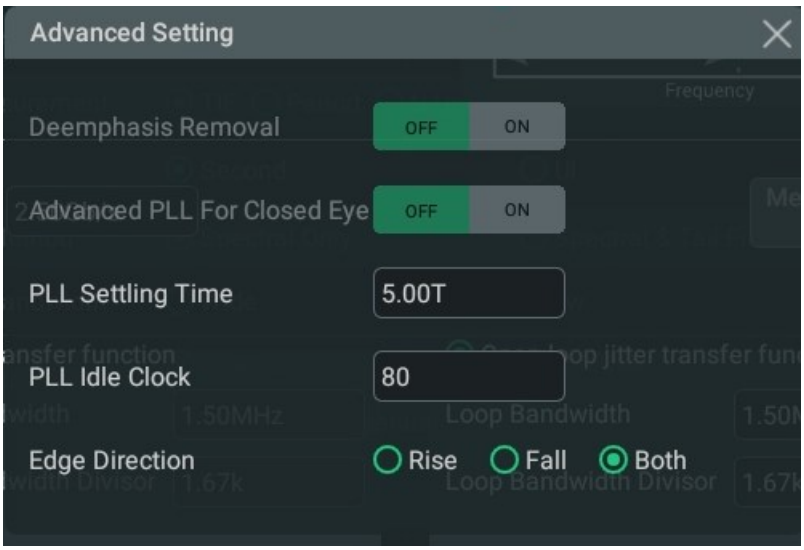
- **Transition Density Dependent**

  The transition density is the rate at which transitions occur within a signal. The transition density of the clock signal is 100%, and it is 50% for the PRBS (Pseudo-Random Binary Sequence) signal. When you enable the transition density dependent, parameters such as loop bandwidth, damping factor, and other parameters of PPL will be affected.

  - OFF: The response of the PLL is static, irrelevant of the transition density.
  - ON: The response of the PLL depends on the transition density, and varies with the transition density.

- **Advanced Setting**

Click or tap **Advanced Setting** to enter the advanced setting interface, as shown in the figure below.



➢ **PLL Settling Time**

Sets the number of clock cycles required for PLL to reach a steady state. The basic jitter measurement and analysis will not be performed for data within the PLL settling time. By default, it is 5T. Increasing this value improves locking reliability, but reduces the amount of effective data to be analyzed.

➢ **PLL Idle Clock**

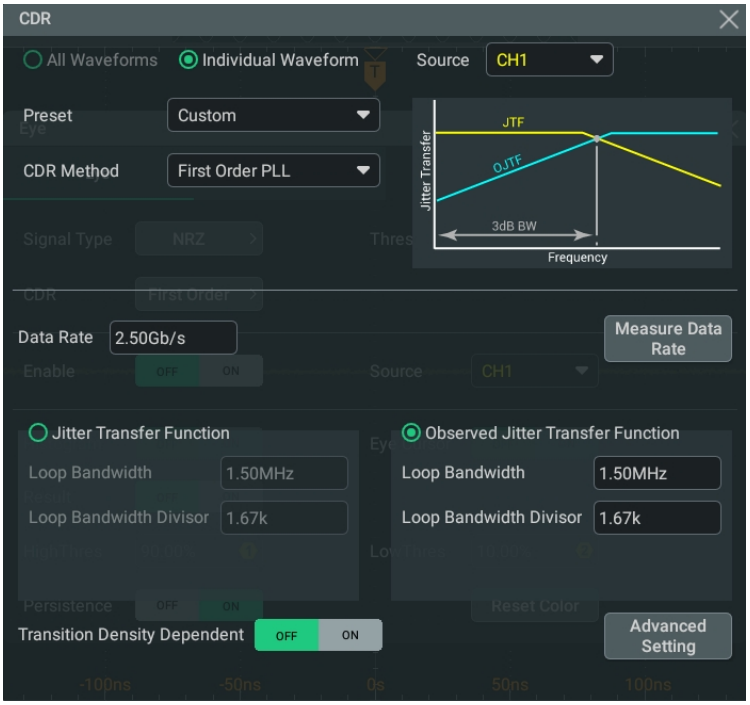
Sets the number of clock cycles required to qualify an idle state. The default value is 80. By default, when no transitions occur for 80 consecutive clock cycles, the PLL enters an idle state and suspends locking; upon detecting a new edge, the PLL initializes and restarts the locking process.

➢ **Edge Direction:** Same as the one defined in "Constant Frequency".

"Deemphasis Removal" and "Advanced PLL for Closed Eye" are not supported currently.

3.3.2.2 First Order PLL

When you select "First Order PLL", the following interface is displayed, as shown below.



The available jitter transfer functions for PLL is as follows:

- **Jitter Transfer Function (JTF)**

  It typically exhibits a low-pass characteristic: low-frequency jitter components (below the loop bandwidth) are tracked and transferred by the PLL, while high-frequency jitter components (above the loop bandwidth) are rejected and filtered out.

- **Observed Jitter Transfer Function (OJTF)**

  This function has a high-pass effect, complementary to JTF. The mathematical relationship is shown in the formula: OJTF = 1 - JTF.

Two configuration parameters are available for the First Order PLL.

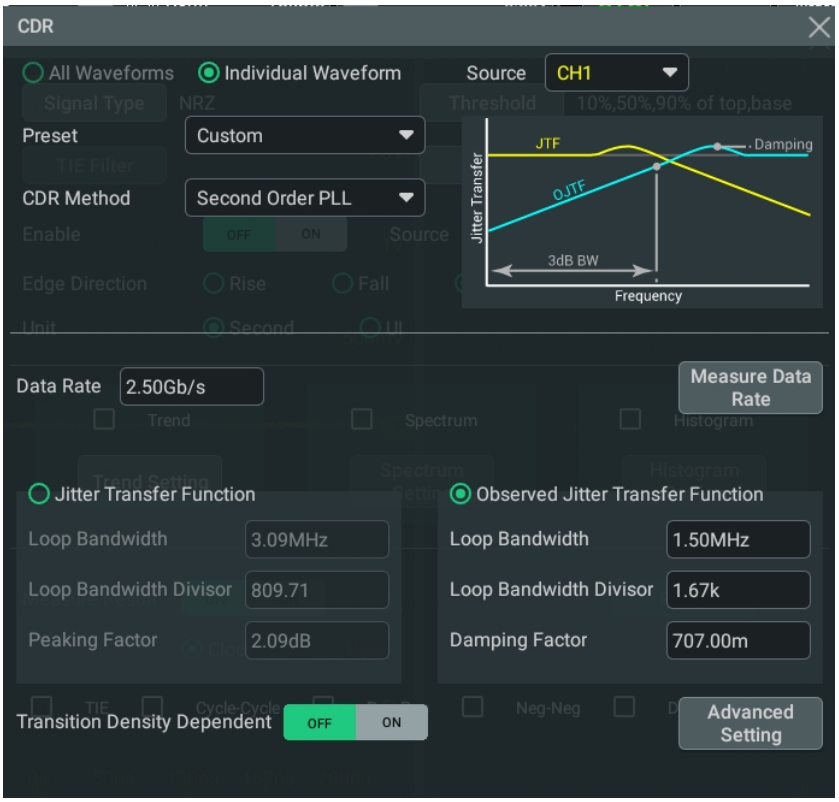
- **Loop Bandwidth:** The unit is Hz. The larger the bandwidth value, the shorter the settling time, the worse the anti-interference.
- **Loop Bandwidth Divisor:** No-scale parameter. It indicates the proportion **of the** loop bandwidth to the data rate.

Relationship between the data rate and the PLL parameter: **Data Rate** = **Loop Bandwidth** x **Loop Bandwidth Divisor**

Modifying either one of the parameters (Loop Bandwidth or Loop Bandwidth Divisor), the other one will change with it.

3.3.2.3 Second Order PLL

When you select "Second Order PLL", the following interface is displayed, as shown below.



The configuration parameters for the Second Order PLL is essentially the same as that for the First Order PLL, but two more parameters are added.

- **Peaking Factor**

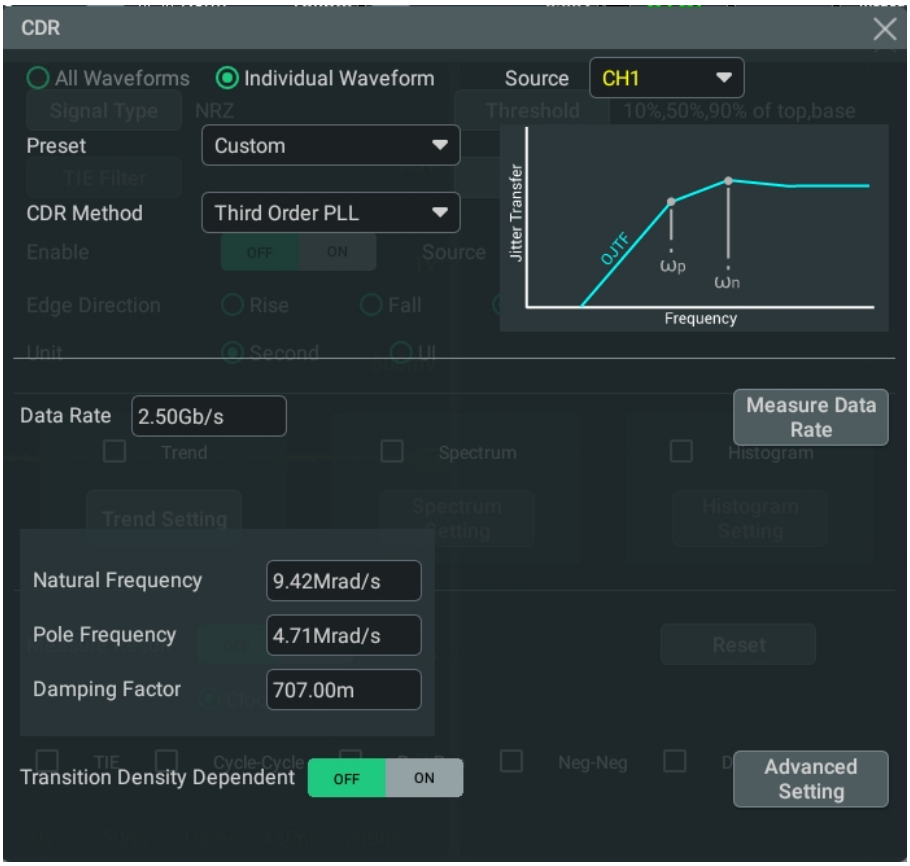
  The maximum PLL gain applied to jitter components at a specific frequency, expressed in dB. The larger the peaking factor value, the shorter the PLL settling time, the worse the anti-interference.

- **OJTF Damping Factor**

  It is inversely proportional to the JTF peaking factor. It is unitless, ranging from 0 to 1. By default, it is 0.707 (707.00m).

3.3.2.4 Third Order PLL

When you select "Third Order PLL", the following interface is displayed, as shown below.



- **Natural Frequency (ω_n)**

  Characterizes the undamped natural frequency of the 3rd-order PLL, in rad/s. The larger the natural frequency value, the shorter the PLL settling time, the worse the anti-interference.

- **Pole Frequency (f_p)**

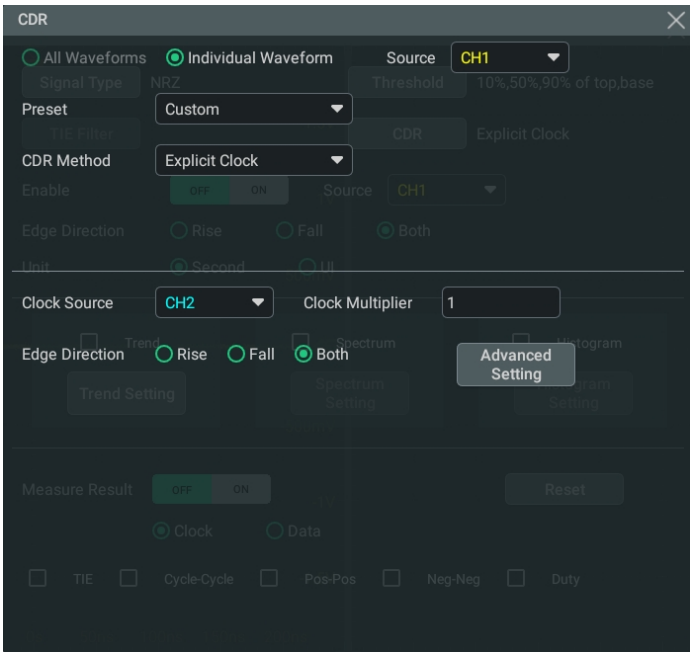
  The frequency corresponding to the pole in the 3rd-order PLL transfer function, in

rad/s. It represents the critical frequency at which high-frequency attenuation becomes significant. When the signal frequency exceeds this pole frequency, the PLL begins to introduce substantial attenuation and phase lag to the signal. The larger the pole frequency value, the shorter the PLL settling time, the worse the anti-interference.

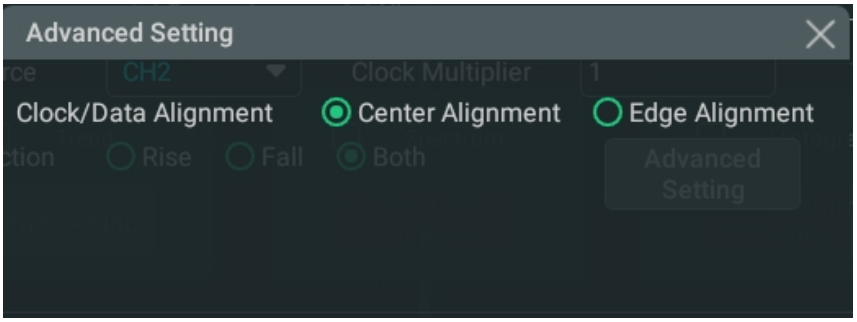
- **Damping Factor (ζ):** Same as what described for the damping factor in the third-order PLL.

3.3.3 Explicit Clock

Directly utilizes an external high-precision reference clock as the data sampling clock for the signal under test. The external clock and the clock of the signal under test shall be strictly synchronized. The configuration interface is shown below.



- **Clock Source:** specifies the input channel for the external clock signal used for clock recovery.
- **Clock Multiplier:** sets the multiplier of the external clock. For example, for a data signal with a data rate of 200 MHz, with the frequency of the external clock 25 MHz, and the edge direction as Both, you need to set the clock multiplier to 4; set the clock multiplier to 8 when you select the rising or falling edge.
- **Edge Direction:** Same as the one defined in "Constant Frequency".
- **Advanced Setting:** The configuration interface is shown below.



Clock/Data Alignment

- **Center Alignment:** By default, it is Center Alignment. Sample the measured signal along the edge of the recovered clock signal to determine the logic level of the signal under test. In the eye diagram generated by the high-speed serial digital signal, the clock edge corresponds to the center of the eye diagram and is therefore called center alignment.
- **Edge Alignment:** If the clock edge and data edge are aligned synchronously, the signal under test cannot be sampled directly along the edge of the clock signal, but will wait for the waveform to reach a specific phase before sampling.

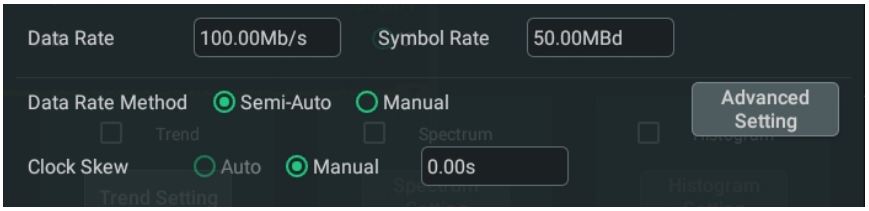
3.3.4 Explicit PLL

The explicit PLL settings have been elaborated in the External Clock and PLL sections, and here will not elaborate more.

3.3.5 PAM Signal Clock Recovery Setting

- **Data Rate**

For PAM signals, the data rate and the symbol rate are not equal, whereas for the NRZ signal, they are the same. Here you can input the symbol rate and data rate separately.



- **Clock Skew**

The clock skew feature of PAM signal clock recovery aligns the center of the eye diagram of the measured signal to the edge of the clock signal by adjusting the phase of the recovered clock signal.

Auto: Not supported. Auto setting for the clock skew does not take effect.

Manual: The oscilloscope adjusts the phase of the recovered clock signal based on the user-defined clock skew value.

3.4 Other Recommended Settings for Clock Recovery

- **Sample Rate:** sets the sample rate to the maximum supported value of the device to ensure accurate capture of the signal edge.
- **Vertical Scale:** adjusts the vertical scale to make the signal amplitude take up the full display area to maximize the measurement resolution.
- **Memory Depth:** sets the memory depth to Auto, and adjusts the horizontal time base for a maximum capture duration.
- **Clock Recovery Algorithm**

  Common Signals: select the default Constant Frequency method, which is applicable to most scenarios.

  Complex Signals: For signals with modulation or significant jitter, we recommend you to select Second Order PLL clock recovery method.

4. Typical Application

The following section takes RIGOL DS9000 series oscilloscope (with JITTA option installed) as an example to introduce how to perform the clock recovery measurement for several typical high-speed serial digital signals.

4.1 Clock Recovery for the NRZ Signal

4.1.1 Constant Frequency

Refer to the following procedure.

Step 1: Input the NRZ signal under test to the specified channel (e.g., CH1) of the oscilloscope.

Step 2: Set "Signal Type" to NRZ, and select CH1 as the source channel.

Step 3: Click or tap **Threshold** to enter the threshold setting interface. Click or tap the drop-down button of **Threshold** to select **10%, 50%, 50% of top, base**. Set **Level Setting** to Default.

Step 4: Click or tap **CDR** to enter the CDR interface. Click or tap the drop-down button of **CDR Method** to select **Constant Frequency**. Set **Data Rate Method** to Auto.

Step 5: Click or tap **Advanced Setting** to enter the advanced setting interface. Click or tap Both for **Edge Direction**.

Step 6: The configuration is complete.

4.1.2 Second Order PLL

Refer to the following procedure.

Step 1: Input the NRZ signal under test to the specified channel (e.g., CH1) of the oscilloscope.

Step 2: Set "Signal Type" to NRZ, and select CH1 as the source channel.

Step 3: Click or tap the "Threshold" menu to enter the threshold setting interface. Click or tap the drop-down button of **Threshold** to select "**threshold+/-hysteresis**". Click or tap **AutoSet**.

Step 4: Click or tap CDR to enter the CDR interface.

Click or tap the drop-down button of **CDR Method** to select "Second Order PLL".

Input the expected data rate; also you can click or tap Measure Data Rate to auto adjust the data rate.

Click or tap to select "Observed jitter transfer function", and then set "Loop Bandwidth Divisor" to 1666.67, and set "Damping Factor" to 0.707.

Disable "Transition Density Dependent".

Step 5: Click or tap **Advanced Setting** to enter the advanced setting interface. Click or tap Rise for **Edge Direction**. By default, PLL Settling Time is 5T, and PLL Idle Clock is 80.

Step 6: The configuration is complete.

4.1.3 Explicit Clock

Refer to the following procedure.

Step 1: Input the NRZ signal under test to CH1, and input the external clock signal to CH2 of the oscilloscope.

Step 2: Set "Signal Type" to NRZ, and select CH1 as the source channel.

Step 3: Click or tap Threshold to enter the threshold setting interface. Set the threshold for the clock channel and the data channel respectively. Select "Individual Waveform" and set the source to CH1.

Step 4: Click or tap CDR to enter the CDR interface. Click or tap the drop-down button of **CDR Method** to select "Explicit Clock". Click or tap the drop-down button of **Clock Source** to CH2. Set "Edge Direction" and "Clock Multiplier" of the external clock signal based on the actual test requirements.

Step 5: Click or tap **Advanced Setting** to enter the advanced setting interface. Click or tap to select the mode of the Clock/Data Alignment.

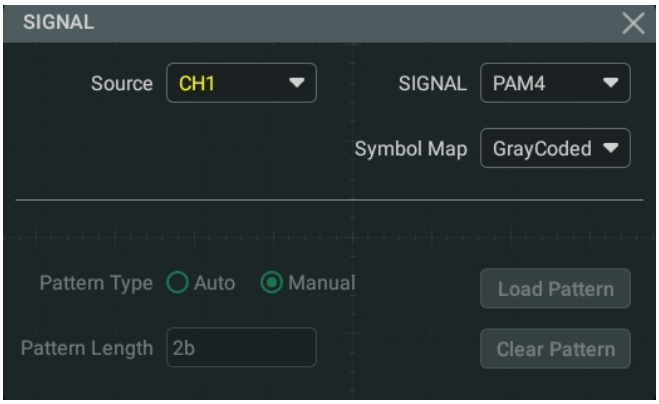
Step 6: The configuration is complete.

4.2 Clock Recovery for the PAM Signal

The difference for the clock recovery settings for the PAM signal and the NRZ signal lies in their threshold settings. Here we take semi-automatic constant clock recovery as an example to illustrate the typical settings for the PAM signal.

Step 1: Input the PAM4 signal under test to CH1 of the oscilloscope.

Step 2: Set "Signal Type" to PAM4, and select CH1 as the source channel.



Step 3: Click or tap **Threshold** to enter the threshold setting interface. Click or tap the drop-down button of **Threshold** to select **50% of levels**. Set **Level Setting** to "PAM Auto Level".

Step 4: Click or tap **CDR** to enter the CDR interface. Click or tap the drop-down button of **CDR Method** to select **Constant Frequency**. **Set the data rate or symbol rate for the PAM signal.** Clock Skew is not required to be set.

Step 5: Click or tap **Advanced Setting** to enter the advanced setting interface. Click or tap Both for **Edge Direction**.

Step 6: The configuration is complete.

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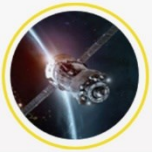

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